REMARKS

Reconsideration of the above-identified application, as amended, is respectfully requested.

In the present Official Action, the Examiner first objected to Claim 9 as allegedly comprising an informality as being of improper dependent form as failing to further limit Claim 1 from which it depends. Further Claim 9 was rejected under 35 U.S.C. §112, second paragraph, as being indefinite for allegedly failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. It is alleged that Claim 9 provides a broad definition of a range/limitation that is dependent upon a claim (Claim 1) having a narrower statement of the range/limitation.

In response to both of these rejections, Claim 9 is being amended to set forth that the blocking impurity is C, singly or in combination with said Sn or Pb. Thus, Claim 9 as amended, further narrows Claim 1 in a manner that avoids the indefiniteness.

Accordingly, the Examiner is requested to withdraw the rejection and objection to Claim 9, as now amended.

Further in the Office Action, the Examiner rejected the Claims 1, 2 and 4-9 under 35 U.S.C. §103(a) as allegedly being unpatentable over Xiang (U.S. Patent No. 6,849,527)("Xiang") in view of Noda et al. (U.S. Patent No. 6,432,802)("Noda").

In response to the rejection of Claims 1, 2 and 4-9 under 35 U.S.C. §103(a) as being unpatentable over Xiang in view of Noda, Applicants respectfully disagree.

With respect to Claim 1, applicants amend the claim to set forth a semiconducting field-effect transistor device comprising:

a first strained layer of semiconductor material doped of a first dopant type formed on a substrate;

a source region and a drain region implanted with dopants of a second opposite type;

a gate electrode separated from the first layer by a dielectric region, and positioned between said source and drain regions;

said substrate having one or more threading dislocations, misfit dislocations or crystal defects that extend continuously from the source region to the drain region at an interface between said first strained layer of semiconductor material and said substrate, and

blocking impurity dopant materials selected from the group comprising: In, Pb, Sb and Sn, that partially or fully occupies each said one or more threading dislocations, misfit dislocations or crystal defects along said interface, wherein said blocking impurity dopant materials substantially inhibit diffusion of said implanted source and drain dopants from diffusing along said threading dislocations, misfit dislocations or crystal defect along said interface.

Respectfully, no new matter is being added and full support is found in the specification (e.g., at paragraphs [0022] as originally filed) which describes misfit locations 140 (in Fig. 3) that extend along the substrate (Si)/SiGe interface and the atoms (e.g., In atoms 190) that block atoms along the dislocation (i.e., along the interface).

In the present invention, it is clear that the semiconducting substrate of the FET device claimed has one or more threading dislocations, misfit dislocations or crystal defects that extend continuously from the source region to the drain region along an interface between a first strained layer of semiconductor material and the substrate, and that blocking impurity dopant materials selected from the group comprising: In, Pb, Sb and Sn, are provided that

partially or fully occupies each said one or more threading dislocations, misfit dislocations or crystal defects along the interface, wherein said blocking impurity dopant materials substantially inhibit diffusion of said implanted source and drain dopants from diffusing along said threading dislocations, misfit dislocations or crystal defect along the interface.

Xiang respectfully, only teaches use of a Carbon impurity implanted in a device active region for purposes of enhancing carrier mobility in that region. That is, Xiang is only concerned with matching hole mobility in a PMOS device to balance an amount of hole mobility provided with a corresponding connected NMOS device. The purpose of Xiang's impurity implantation is to change the lattice spacing within the strained silicon lattice of a device channel to impart additional strain to bolster the hole minority carrier in the PMOS device channel.

This is very different from the present invention as follows:

1. Xiang does not teach nor suggest use of such impurity implants to perform a blocking function. In fact, Xiang teaches away from the teachings of Claim 1, as amended, as impurities are implanted in the strained layer portion of the device channel region per se (See Xiang at Fig. 3c) to increase the level of strain and hence, carrier mobility, and does not teach or suggest blocking impurity dopant materials that partially or fully occupy threading dislocations, misfit dislocations or crystal defects along an interface between a first strained layer of semiconductor material and the substrate.

2. Xiang does not teach impurity dopant materials selected from the group comprising: In, Pb, Sb and Sn, that partially or fully occupies each said one or more threading dislocations, misfit dislocations or crystal defects along the interface between a first strained layer of semiconductor material and the substrate.

3. Xiang's and Noda's teaching of use of halo regions is not suggestive of the inventive implantation of impurity dopant materials selected from the group comprising: In, Pb, Sb and Sn, that partially or fully occupies each said one or more threading dislocations, misfit dislocations or crystal defects along the interface between a first strained layer of semiconductor material and the substrate. Halo implantations are doped regions that help suppress short channel "punchthrough" effect by shortening the depletion regions at the *ends of the source and drain regions* and are only formed at *opposing sides* of a device channel to prevent source/drain dopant diffusion into the "channel region". To the contrary, in the present invention, impurity dopant materials are implanted to partially or fully occupy each said one or more threading dislocations, misfit dislocations or crystal defects along the interface between a first strained layer of semiconductor material and the substrate (and NOT at opposing sides of a device channel).

4. Notwithstanding Noda's teaching of using In, Pb, Sb and other impurities besides Carbon (which is taught in Xiang only for purposes of enhancing the strain of a Si-based layer in the channel region), again Xiang's and Noda's dopant implantation structures are to provide source/drain halo regions which, structurally, are at opposing

sides of a channel and only for purposes of preventing diffusion of dopants into a device channel region per se. This is not a teaching of a structure having impurity dopant materials implanted to partially or fully occupy each said one or more threading dislocations, misfit dislocations or crystal defects along the interface between a first strained layer of semiconductor material and the substrate to substantially inhibit diffusion of said implanted source and drain dopants from diffusing along said threading dislocations, misfit dislocations or crystal defect along the interface.

For these reasons, Xiang, whether taken alone or in combination with Noda, does not render Claim 1 as amended unpatentable as neither Xiang (nor Noda) teaches use of a blocking impurity dopant material that partially or fully occupies each said one or more threading dislocations, misfit dislocations or crystal defects along an interface between a first strained layer of semiconductor material and the substrate, as recited in amended Claim 1. Claim 1 as amended includes the implantation of blocking impurities NOT in a halo region abutting the source and drain dopant regions, but along the interface between the first strained layer and the substrate - thereby substantially inhibiting diffusion of implanted source and drain dopants from diffusing along said threading dislocations, misfit dislocations or crystal defect along said interface. That is, the present invention does not utilize halo extensions nor is relying on any teaching thereof.

Thus, since each and every limitation within applicant's invention as disclosed and claimed within amended claim 1 is not taught in Xiang, either expressly or inherently, whether taken alone or in combination with Noda, applicant asserts that claim 1 may not

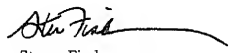
properly be rejected under 35 U.S.C. §103(a) as being unpatentable over Xiang in view of Noda. Due to their dependency upon claim 1, applicant also asserts that claims 2, and 4 - 9 may also not properly be rejected under 35 U.S.C. §103(a) by virtue of their dependency upon Claim 1 as amended. As such, the Examiner is respectfully requested to withdraw the rejection of Claims 1, 2 and 4-9 under 35 U.S.C. §103(a).

With respect to the rejections of Claims 5 and 6, as allegedly unpatentable over Xiang in view of Noda, applicants respectfully disagree. Xiang teaches use of halo extensions as generally known to encompass the source and drain diffusions. Noda, while teaching implantation of specific heavy ions, e.g., Indium, is for the purpose of forming a diffusion pocket layer that, as shown in every figure of Noda, is formed beneath the source and drain diffusion regions at opposing sides of the channel. Noda is not even directed to strained-Si substrates and does not address the same problem as Xiang relating to enhancing mobility of carriers in the channel regions to counteract effects of stress/strain. Thus, as neither Noda nor Xiang teach or suggest the implantation of blocking impurity dopant materials selected from the group comprising: In, Pb, Sb and Sn, provided to partially or fully occupy each said one or more threading dislocations, misfit dislocations or crystal defects along the interface between a first strained layer and the substrate, to substantially inhibit diffusion of said implanted source and drain dopants from diffusing along said threading dislocations, misfit dislocations along the interface, Applicants respectfully submit that Claims 5 and 6 can not be rejected under 35 U.S.C. §103(a) as being unpatentable over Xiang in view of Noda.

As such, the Examiner is respectfully requested to withdraw the rejection of Claims 5 and 6 under 35 U.S.C. §103(a).

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance. Accordingly, it is respectfully requested that this application be allowed and a Notice of Allowance be issued. If the Examiner believes that a telephone conference with the Applicants' attorneys would be advantageous to the disposition of this case, the Examiner is requested to telephone the undersigned, Applicants' attorney, at the following telephone number: (516) 742-4343.

Respectfully submitted,



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